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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,238	01/29/2004	Toshitake Yaegashi	81790.0311	6199

26021 7590 05/02/2005

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EXAMINER	
WILSON, ALLAN R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/768,238	YAEGASHI ET AL.	
	Examiner	Art Unit	
	Allan R. Wilson	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/112,482.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/29/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 17-20 are rejected under 35 USC § 102(b) as being anticipated by Japanese Patent Application No. 8-23041 ("JP '041") disclosed by Applicants.

With regards to claim 17, JP '041 illustrates in figures 1-17, particularly figures 1-7, (entire document) forming, on a first region 5 of a semiconductor substrate 1, a self-aligned double-layer gate structure which includes a gate insulating film 10, a first conductor 11 serving as a floating gate layer, a second conductor 13 serving as a control gate layer, and an insulating film 12 electrically insulating the first and second conductors,

patterning the first conductor into a gate electrode of a transistor above a second region 6 of the semiconductor substrate; and

providing a third conductor 21 on the first conductor patterned in a form of the gate electrode above the second region.

With regards to claim 18, JP '041 illustrates in figs. 1-7 sequentially forming, on a semiconductor substrate 1, a gate insulating film 10, a first conductor 11 serving as a floating gate layer, an insulating film 12, and a second conductor 13 serving as a control gate layer;

patterning the second conductor, the insulating film and the first conductor in a self-aligned manner in a first region 5 of the semiconductor substrate, using a single mask, thereby forming a double-layer gate structure (fig. 3), and removing that portion of the second conductor which is provided on a second region of the semiconductor substrate during the patterning of the second conductor in the first region (fig. 4);

forming a third conductor 21 on the first conductor in the second region 6 after the patterning of the first conductor in the first region, such that the first and third conductors are electrically connected to each other; and

patterning the third and first conductors into a gate electrode of a transistor in the second region.

With regards to claims 19 and 20, JP '041 illustrates in figs. 1-7 forming an element isolating region 3 (in region 5) adjacent to the transistor, and forming the double-layer gate structure on the element isolating region.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Kono et al. and Mazzali (illustrate a memory device with dual gate and single gate transistors).

Field of Search	Date
U.S. Class and subclass: 257/201, 211, 257, 275	April 29, 2005
Other Documentation: None	N/A
Electronic data base(s): EAST (USPAT, US-PGPUB, JPO, EPO, Derwent, IBM TDB)	April 29, 2005

Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone number is (571) 272-1738. Examiner Wilson can normally be reached 7:00-4:00 Monday-Thursday and 6:00-3:00 on Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Allan R. Wilson
Primary Examiner
29 April 2005